REMARKS

This responds to the Office Action dated January 3, 2005. Claims 5, 25, 32 and 37 are amended, claims 11, 29 are canceled; as a result, claims 1-10, 12-28, and 30-40 are now pending in this application.

§102 Rejection of the Claims

Claims 5-29 were rejected under 35 USC § 102(e) as being anticipated by Chehrazi et al. (U.S. 6,301,599, "Chehrazi").

Regarding claims 5-10,12:

Applicant is unable to find in Chehrazi, among other things,

> a plurality of logic circuits coupled to ones of said plurality of transistors to output Booth encoded signals, wherein said Booth encoded signals are substantially delay-matched at an output of said Booth encoder circuit,

as presently recited or incorporated in the claims. The cited portions of Chehrazi refer to a critical path which exhibits a delay equivalent to approximately four NAND gates (see col. 8, claim 13), and Chehrazi defines the critical path as the logical flow through a circuit which takes the longest time to complete (see col. 1, lines 65-67). Therefore, the cited portions of Chehrazi do not refer to Booth encoded signals which are substantially delay-matched at an output.

Regarding claims 13-21:

Applicant is unable to find in Chehrazi, among other things, logic configured to have a maximum of three gate delays from an input of said multiplier circuit to an output of said multiplier circuit, as recited or incorporated in the claims. The cited portions of Chehrazi refer to a critical path which encounters a delay approximately equivalent to four NAND gates (see col. 6, lines 63-65, and Figs. 4 and 5), and Chehrazi defines the critical path as the logical flow through a circuit which takes the longest time to complete (see col. 1, lines 65-67).

Regarding claims 22-24:

Applicant is unable to find in Chehrazi, among other things,

> logic including a plurality of transistors, a plurality of NAND gates and a plurality of inverters configured to output delay-matched Booth encoded signals based on said multiplier bits and said complements,

as recited or incorporated in the claims. The cited portions of Chehrazi refer to a critical path which encounters a delay approximately equivalent to four NAND gates (see col. 6, lines 63-65, and Figs. 4 and 5), and Chehrazi defines the critical path as the logical flow through a circuit which takes the longest time to complete (see col. 1, lines 65-67). Therefore, the cited portions of Chehrazi do not refer to output delay-matched Booth encoded signals.

Regarding claims 25-28:

Applicant cannot find in the cited portions of Chehrazi, among other things, wherein said Booth encoded signals are substantially delay-matched at an output of said Booth encoder circuit, as presently recited or incorporated in the claims. Additionally, Applicant cannot find said second subcircuit to provide a signal to second logic circuits, or said third subcircuit to provide a signal to third logic circuits, as recited or incorporated in the claims. The Office Action only refers to logic circuits S2 and S_2 in Fig. 4 of Chehrazi.

Applicant respectfully requests reconsideration and allowance of claims 5-10 and 12-28.

Claims 30-31 and 33-40 were rejected under 35 USC § 102(b) as being anticipated by Lee et al. (U.S. 5,818,743, "Lee"). Applicant respectfully traverses the rejection.

Regarding claims 30-31 and 33-36:

Applicant is unable to find in Lee, among other things,

> a second multiplexing device having a plurality of second transistors to receive said Booth encoded signals and multiplexed data from said first multiplexing device and to provide a second partial products output,

as recited or incorporated in the claims. The MUX devices in Lee, that are referred to at the bottom of page 68 of the Office Action, apparently receive inputs from Full Adders (see Fig. 9A and col. 6 lines 38-49) rather than Booth encoded signals and multiplexed data, as claimed.

Regarding claims 37-40:

Applicant is unable to find in Lee, among other things,

> a multiplexing device to receive Booth encoded signals and to provide a first partial product output for a first bit of a multiplicand based at least on multiplexed data received from a previous multiplexing device,

as presently recited or incorporated in the claims. The MUX devices in Lee apparently receive inputs from Full Adders (see Fig. 9A and col. 6 lines 38-49).

Applicant respectfully requests reconsideration and allowance of claims 30-31 and 33-40.

§103 Rejection of the Claims

Claims 1-4 were rejected under 35 USC § 103(a) as being obvious over Chehrazi et al. (U.S. 6,301,599) in view of Lee et al. (U.S. 5,818,743). Applicant respectfully traverses the rejection.

In order to establish a *prima facie* case of obviousness the cited reference or references must teach or suggest all the claim limitations. *M.P.E.P. 2143.03.* Applicant is unable to find in the proposed combination of Chaharzi and Lee a teaching or suggestion of, among other things,

> a partial products generating circuit having a first multiplexing device to receive said Booth encoded signals and to provide a first partial products output, and a second multiplexing device to receive said Booth encoded signals and multiplexed data from said first multiplexing device and to provide a second partial products output,

as recited or incorporated in the claims. The MUX devices in Lee, that are referred to at the bottom of page 8 of the Office Action, apparently receive inputs from Full Adders (see Fig. 9A and col. 6 lines 38-49). Applicant respectfully requests reconsideration and allowance of claims 1-4.

Claim 32 was rejected under 35 USC § 103(a) as being obvious over Lee et al. (U.S. 5,818,743). Applicant respectfully traverses the rejection.

Claim 32 depends on base claim 30 and incorporates all the elements of the base claim. Applicant is unable to find in Lee a teaching or suggestion of all elements of the contested claims as discussed above in regard to claim 30. Claim 32 is amended to respond to the indicated informalities and not to distinguish the claim over the subject matter in Lee. Applicant respectfully requests reconsideration and allowance of claim 32.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6970) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date March 22, 2005

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of March, 2005.

Amy Moriarty
Name

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Signature